

# SG16080A (160 DOTS X 80 DOTS )

## FEATURES

- ◆ NO BUILT- IN CONTROLLER
- ◆ 2.7~5.5V POWER SUPPLY
- ◆ 1/128 DUTY CYCLE
- ◆ 8-BIT PARALLEL INTERFACE

## MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size (W x H x T)	109.0 x 73.0 x 10.2	mm
Viewing Area ( W x H )	77.5 x 54.0	mm
Active Area ( W x H )	70.36 x 47.16	mm
Dot Size ( W x H )	0.4 x 0.55	mm
Dot Pitch ( W x H )	0.44 x 0.59	mm

## INTERFACE PIN CONNECTIONS

NO.	SYMBOL	LEVEL	FUNCTION
1~4	DB0-DB3	H/L	Data Bus Line
5	/DispOFF	H/L	Display OFF.Active LOW
6	FRM	H	Frame start signal
7	LEDOFF	L	Power Supply For LED
8	CL1	H→L	Common Driver Data Shift Signal
9	CL2	H→L	Clock Pulse For Segment Shift Register
10	V <sub>DD</sub>	5V	Power Supply Voltage
11	V <sub>SS</sub>	0V	Power Supply Ground
12	V <sub>EE</sub>	-	Power Supply Voltage For LCD
13	V <sub>o</sub>	-	Contrast Adjustment Voltage
14	FGND	-	Frame Ground
15	A	3.4V	LED Power (+)
16	K	0V	LED Power (-)

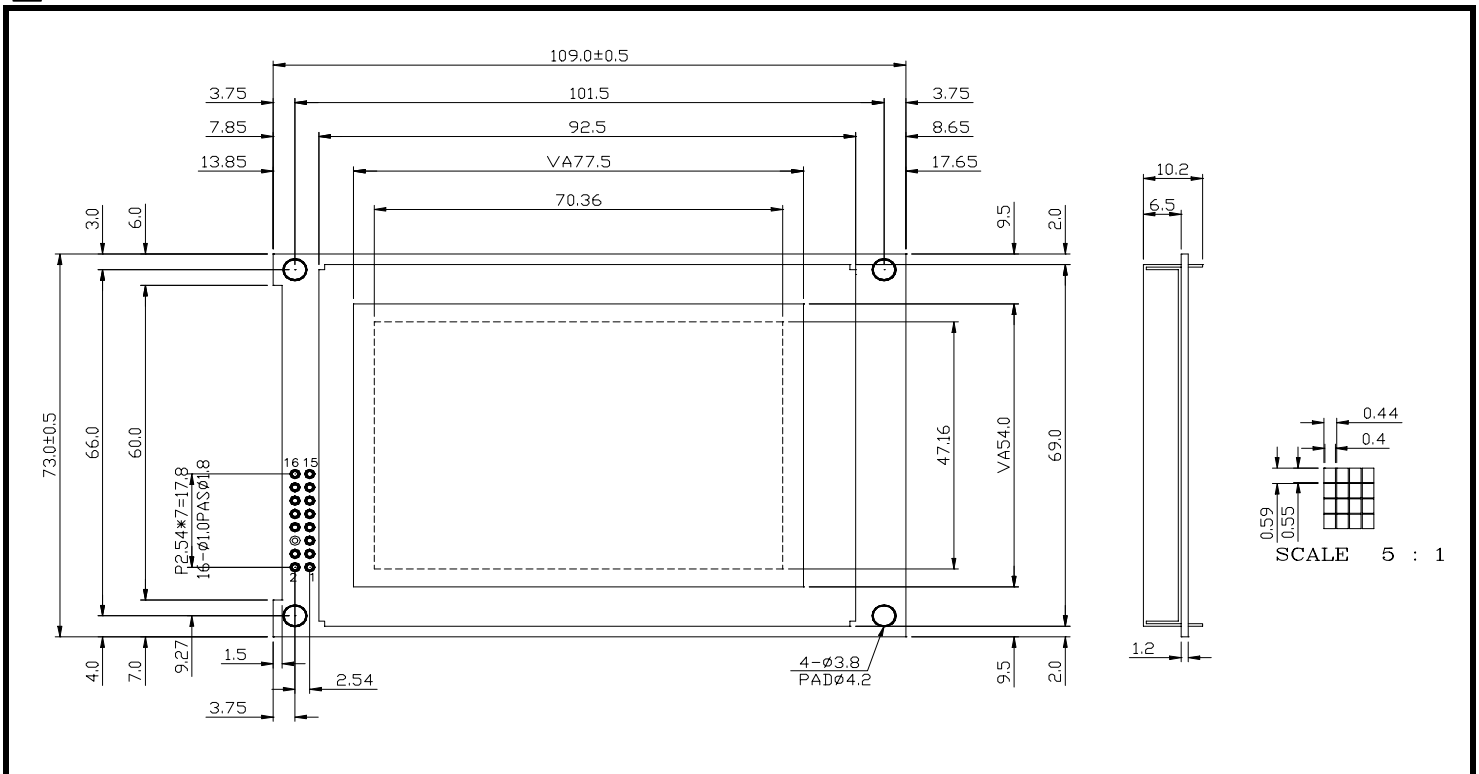
## ABSOLUTE MAXIMUM RATINGS

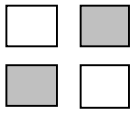
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V <sub>DD</sub> -V <sub>SS</sub>	0	-	7	V
Supply Voltage For LCD Drive	V <sub>DD</sub> -V <sub>o</sub>	0	-	28	V
Input Voltage	V <sub>I</sub>	V <sub>SS</sub>	-	V <sub>DD</sub>	V

## ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage For Logic	V <sub>DD</sub> -V <sub>SS</sub>	-	2.7	5	5.5	V	
LCD Supply Voltage	V <sub>DD</sub> -V <sub>o</sub>	V <sub>DD</sub> =5V Ta=25°C	11.3	12.6	13.8	V	
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> =5V	-	20	30	mA	
Input Voltage	"HIGH" Level	V <sub>IH</sub>	-	2.2	-	V <sub>DD</sub>	V
	"LOW" Level	V <sub>IL</sub>	-	-	-	0.6	V
Output Voltage	"HIGH" Level	V <sub>OH</sub>	-	2.4	-	-	V
	"LOW" Level	V <sub>OL</sub>	-	-	-	0.4	V

## EXTERNAL DIMENSIONS

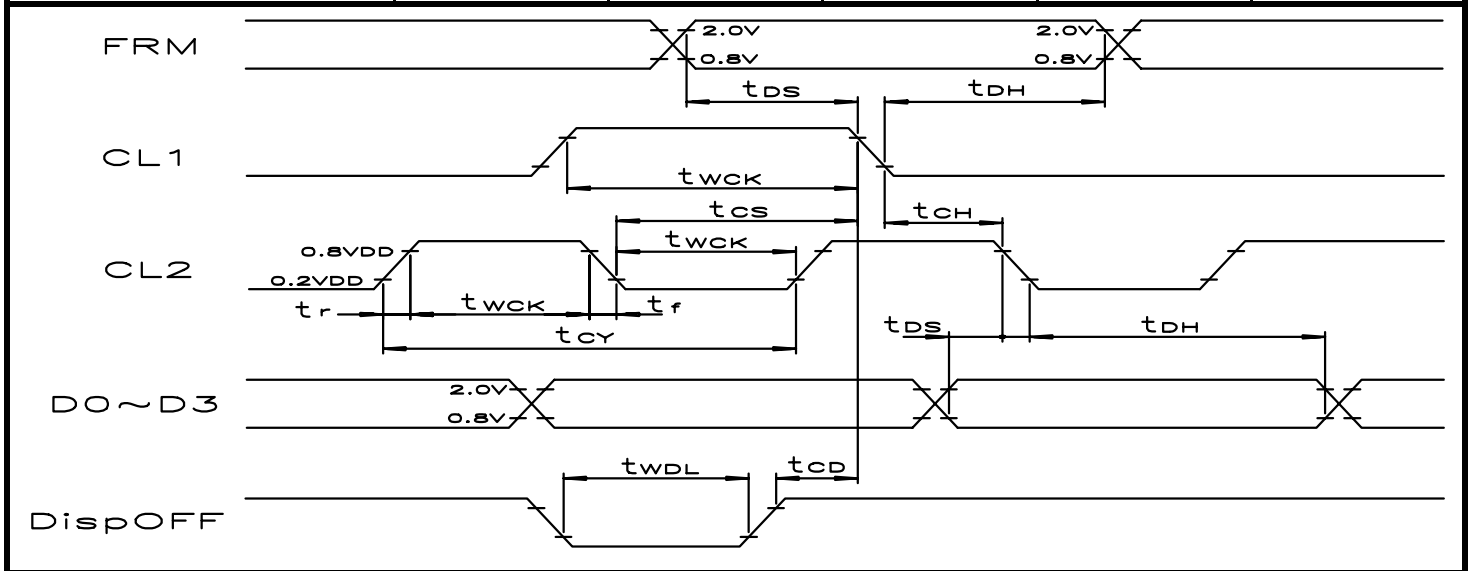




# SG16080A ( 160 DOTS X 80 DOTS )

## TIMING CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT.
Clock cycle time	$t_{CY}$	Duty=50%	250	-	ns
Clock Pulse Width	$t_{WCK}$		95	-	ns
Data Set Up Time	$t_{DS}$		65	-	ns
Data Hold Time	$t_{DH}$		65	-	ns
Latch pulse 'H' width	$t_{WCK}$		95	-	ns
Input signal Rise/Fall Time	$t_r, t_f$		-	30	ns
Clock Set Up Time	$t_{CS}$		120	-	ns
Clock hold time	$t_{CH}$		120	-	ns
FRM set-up time	$t_{DS}$		30	-	ns
FRM hold time	$t_{DH}$		30	-	ns
DispOFF clear time	$t_{CD}$		100	-	ns
DispOFF 'L' pulse width	$t_{WDL}$		1.2	-	$\mu$ s



## BLOCK DIAGRAM

